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EXAMINER	
WERNER, DAVID N	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,813	RAMAKRISHNAN, LAKSHMANAN	
	Examiner	Art Unit	
	David N. Werner	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-4 and 13-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-12 and 16-20* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is the First Action on the Merits for US Patent Application 10/765,813. Currently, claims 1-20 are pending.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-4 and 13-15, drawn to direct memory addressing, classified in class 710, subclass 22.

II. Claims 5-12 and 16-20, drawn to video decoding, classified in class 375, subclass 240.25.

The inventions are distinct each from the other because of the following reasons:

3. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination can be used for generic data, and is not limited to video data. The subcombination has separate utility such as video decoding.

The examiner has required restriction between combination and subcombination inventions. Where applicant elects a subcombination, and claims thereto are

subsequently found allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

4. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction were not required because the inventions have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Mirut P. Dalal on 10 July 2007, a provisional election was made without traverse to prosecute the invention of invention II, claims 5-12 and 16-20. Applicant must make affirmation of this election in replying to this Office action. Claims 1-4 and 13-15 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Priority

6. Since Applicant desires to call attention to related application 10/735,980, as stated in the interview of 10 July 2007, a specific cross-reference to the prior-filed

application in compliance with 37 CFR 1.78(a)(2)(i) must be included in the first sentence(s) of the specification following the title or in an application data sheet.

Drawings

7. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

8. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: packetized elementary sequence 360, transport header 365a, and transport packet 365b, all mentioned in paragraph [0021] of the specification and expected in figure 1. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as

either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

9. The disclosure is objected to because of the following informalities: in paragraph [0009], line 7, the word "transmit" should be "transmits", in paragraph [0013], line 3, the word "he" should be "the", and paragraph [0029] is a verbatim copy of paragraph [0027] and should be deleted.

Appropriate correction is required.

10. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Automatic Direct Memory Access Engine and Method for Dual Macroblock Row Transfer in a Video Decoder".

Claim Objections

11. Claim 5 is objected to because of the following informalities: in line 4, the phrase "second macroblock" should be "second macroblock row". Appropriate correction is required.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 5, 9-12, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 7,007,031 B2 (MacInnis et al.). MacInnis et al. discloses a memory system and a pipeline for a video decoder. Regarding claim 5, in one embodiment of MacInnis et al., a co-processor operates on two macroblock rows simultaneously (column 13, lines 27-30). As shown in figure 8, core processor 202 receives blocks from two rows, alternating between rows after each block (column 14, lines 1-63). These macroblocks correspond with the claimed "successive portions" of the macroblock rows. Co-processor unit A performs operations on row 0, and co-processor unit B independently performs operations on row 1. The core processor provides a macroblock and a start command to each co-processor unit when available, regardless of the status of the other co-processor unit (column 14, lines 37-63).

Regarding claim 9, figure 2 of MacInnis et al. illustrates a media decoding system that can be used as a video decoder (column 5, lines 20-22). Decoder memory 212 locally stores a data unit containing macroblock information received from main memory (column 6, lines 1-14). This corresponds with the claimed "local buffer". When

decoding system 200 acts as a video decoder, core processor 202, co-processor 206, and accelerators 208 and 210 comprise a chipset that performs picture decoding and decompressing (column 6, lines 15-20). Each component uses decoder memory 212 as a local memory (column 6, lines 52-64). Then, decoder 200 corresponds with the claimed "decompression engine". Bridge module 204 communicates with the local decoder memory 212 and main memory 110, according to instructions from core processor 202 (column 6, lines 46-51). This corresponds with the claimed "extractor". Regarding claim 10, as shown in figure 1 of MacInnis et al., DMA controller 106 controls data transfer between system memory 110 and a local memory in video decoder 116 (column 4, lines 57-64). Then, when core processor 202 in video decoder 116 issues a command to read from system memory 110 to local memory 212 through bridge module 204, it inherently does so through DMA controller 106. Regarding claim 11, core processor 202 acts to direct a pipeline, individually receiving and processing macroblocks one at a time, and storing them in local memory 212. The local memory, in turn, contains a plurality of buffers that each store information for one macroblock between operations (column 7, lines 20-41). In the illustrative example described throughout MacInnis et al., five buffers each store macroblock data during processing. When a buffer becomes free, core processor 202 stores a new macroblock to continue decoding (column 16, lines 15-35). Regarding claim 12, as mentioned previously, local memory 212 contains a plurality of buffers, each of which can store data for a different macroblock simultaneously, and co-processor 206 contains two separate units that can simultaneously decode different macroblocks (column 13, lines 26-35).

Regarding claim 20, digital media system 100 of MacInnis et al. corresponds with the claimed "decoder system", digital video decoder 116 corresponds with the claimed "video decoder", decoder memory 212 corresponds with the claimed "local buffer", bridge 204 corresponds with the claimed "extractor", and DMA controller 106 corresponds with the claimed "direct memory access engine".

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 6-8 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis et al. in view of US Patent 4,599,689 (Berman). Although MacInnis et al. teaches providing portions of two macroblock rows to a video decoder from a memory, it does not disclose particulars of how the memory is addressed. Berman teaches a Direct Memory Address (DMA) control apparatus. Regarding claim 6, in the invention of Berman, to transfer data from a main memory through a DMA, a processor first stores the starting address of the data in the main memory in a current address register in the DMA (column 5, lines 42-46). In a system in which the data is loaded from two multiple locations, in this case, two buffers (column 8, lines 30-36), the start address for each buffer is loaded (column 8, lines 56-58). Regarding claims 7 and 8, the DMA engine loads a word count, specifying the number of words to be transferred from a memory,

with the starting address (column 9, lines 3-20). Data is then sequentially transferred word by word, and the address register and word counter are incremented (column 6, lines 12-14). This sequential transfer of data corresponds with the claimed "providing successive portions".

Regarding claim 16, the system of Berman may be incorporated in DMA controller 106 of MacInnis et al. In this case, the two locations of the macroblock rows in the main memory correspond with the two memory addresses in Berman, and the requests for macroblock portions originate in core processor 202 through bridge 204 in MacInnis et al. Regarding claim 17, in Berman, the two starting addresses are stored in registers (column 6, line 5; column 8, lines 56-58). Regarding claims 18 and 19, as mentioned previously, the DMA control apparatus of Berman increments the address registers one word at a time and provides data for a specified word count.

MacInnis et al. discloses the claimed invention except for details of memory addressing. Berman teaches that it was known to increment an address in a DMA controller during a sequential data transfer. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the DMA control system of Berman into the DMA controller of MacInnis et al., as taught by Berman, since Berman states in column 1, lines 33-59 that such a modification would enable a system to automatically handle a large amount of data transfer from a memory while the main processor performs other operations.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 5,583,572 A (Sumihiro) teaches a video decoding system in which odd and even rows are separated in a memory. US Patent 5,696,698 A (Herluison et al.) teaches a motion compensation system in which two cache memories are used. US Patent 5,870,497 A (Galbi et al.) teaches a video decoder in which a memory controller is discussed in detail. US Patent 6,301,299 B1 (Sita et al.) teaches a memory controller that divides decoded macroblocks into upper and lower half macroblocks for field buffer storage. US Patent 6,829,016 B2 (Hung) teaches a digital camera with a double-buffer system for video playback. US Patent 6,999,091 B2 (Saxena et al.) teaches a system that divides a memory into a series of tiles for quick access via two channels. High Performance Memories (Price) describes a cache memory in which the data in a cache line is associated with its corresponding address in the main memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David N. Werner whose telephone number is (571) 272-9662. The examiner can normally be reached on Monday-Friday from 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on (571) 272-7418. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mehrdad Dastouri

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TC 2600

DNW